

NASA TECH BRIEF

Ames Research Center



NASA Tech Briefs announce new technology derived from the U.S. space program. They are issued to encourage commercial application. Tech Briefs are available on a subscription basis from the National Technical Information Service, Springfield, Virginia 22151. Requests for individual copies or questions relating to the Tech Brief program may be directed to the Technology Utilization Office, NASA, Code KT, Washington, D.C. 20546.

High-Speed Data Word Monitor

The problem:

Digital data that is transmitted by data modems usually is in the form of fixed-length blocks. The blocks contain a synchronization code and, in addition to the actual data, may contain data type codes, source codes, destination codes, serial numbers, and error codes. If the input data rate is lower than the transmission rate, the position in the block that normally contains data is filled with a fixed "filler" pattern. When the receiving terminal equipment fails to process the data, the data transmission equipment is usually considered to be at fault, and it is thus necessary to make a visual examination of any portion of the block, in particular the identification codes discussed above. A high-speed display of the bit pattern is required.

The solution:

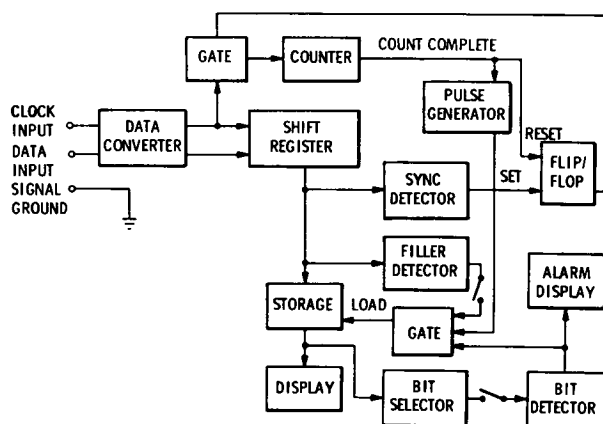
A small, portable, self-contained device that provides a high-speed display of the bit pattern of any selected portion of the transmission, can suppress filler patterns so that the display is not updated, and can freeze the display so that a specific event may be observed in detail.

How it's done:

As indicated in the diagram, bilevel standard clock and data signals are first converted to standard digital logic levels. The serial data stream is then applied to a 24-bit serial-to-parallel shift register and compared in a digital comparator to the synchronization code. When a synchronization code is detected, a divide-by-N counter is started and pulses are counted until a selected event is reached; at this time, the data shift register contains the selected 24-bit word. Then the counter is stopped and the 24-bit latch is enabled.

thus holding and displaying the selected word. The divide-by-N counter is programmed by panel switches.

When a fixed filler pattern is decoded and enabled on the front panel, updating of the display is inhibited



so that the selected data word can be observed continuously. Additionally, a stop-bit select switch will inhibit display update when one selected bit in the 24-bit word changes from a logical "zero" to a logical "one," so that a specific event, such as the presence of an error status code, can be observed. In this instance, the display can be updated again by a panel switch.

Note:

No additional documentation is available. Specific questions, however, may be directed to:

Technology Utilization Officer
Ames Research Center
Moffett Field, California 94035
Reference: B75-10129

(continued overleaf)

Patent status:

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning non-exclusive or exclusive license for its commercial development should be addressed to:

NASA Patent Counsel
Mail Code 200-11A
Ames Research Center
Moffett Field, California 94035

Source: Manfred N. Wirth
Ames Research Center
(ARC-10899)